

(SYLLABUS)

1.

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| (Course Title) | | (Instructor) | | | |
| (Year) | 2023 | (Semester) | 1 | (Course No.) | 2150098801 |
| (Class) | 01 | (Open to) | | (Course Classification) | - |
| (Credit) | 3.0 | | 03 | | Pass/Fail |
| | | | | | |
| (Office) | 203 | (Telephone) | 02-829-8228 | (e-mail) | mju20@ssu.ac.kr |
| | | | | | |
| | (*) (ABEEK Classification) | | (*) (ABEEK Requirement) | | |
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| (Course Description) | CIS SK 가 | | | | |

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| (Required Texts) | | * /SK |
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| | 70% 70% Pass | |

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2.

| (Week) | (Keyword) | (Description) | | (Texts) |
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| 01 | Overview | - 25 - ? - 가 ? | | |
| 02 | DRAM (1) | - CMOS Logic - Logic (가 -) - DRAM | | |
| 03 | DRAM (2) | - DRAM - DRAM Core (Active / Read / Write / Precharge) - DRAM Addressing - Package | | |
| 04 | NAND (1) | - NAND Cell Array - NAND Flash - NAND Block NAND Addressing | | |
| 05 | NAND (2) | - NAND operation (Read/Program/Erase) | | |
| 06 | NAND (3) | - Multi Plane Operation - Cache Operation, Plane Interleave - Suspend, SPO, Summary - NAND! | | |
| 07 | DRAM (1) | - DRAM - DRAM | | |
| 08 | DRAM (2) NAND (1) | - DRAM Process Integration - NAND Basic Operation Structure | | |
| 09 | NAND (2) | - 3D NAND Bit Growth - Characteristics Reliability | | |
| 10 | Solution (1) | - Solution - SoC - SoC | | |
| 11 | Solution (2) | - FW ? - HIL - FTL : ATL, VFL | | |
| 12 | Solution (3) | - Solution - Solution - Solution | | |
| 13 | | - / Overview - - - DRAM Test | | |
| 14 | CIS Overview | - CIS / - CIS - ISP 가 - CIS /CIS | | |
| 15 | | - Keywords - AIM | | |

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| | Open-ended problem | | |
| | Teamwork | | |
| | Communication skills | | |